VFE Calibration – Pedestals and Bad Channels in the VFE Electronics

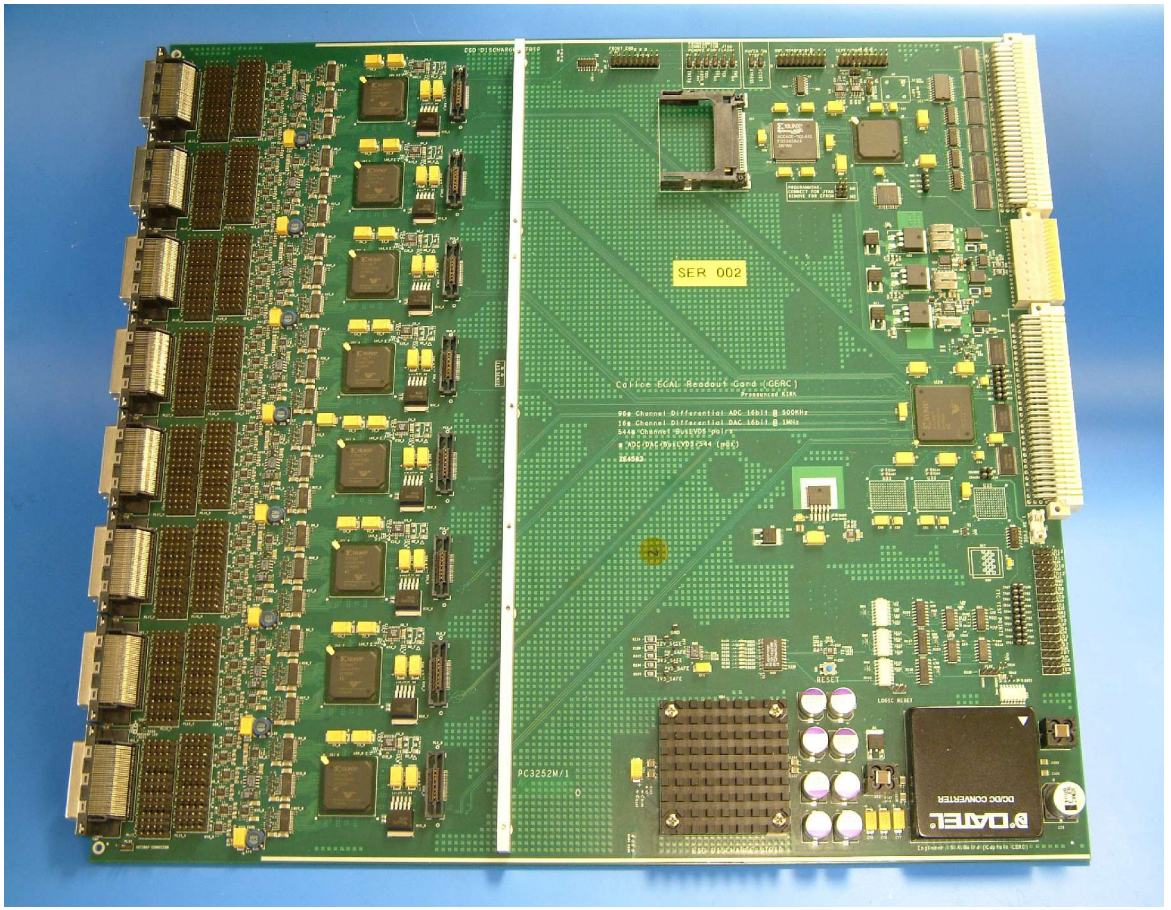
Christopher Targett-Adams

CALICE Test-Beam Meeting, Monday, 6th March 2006

Contents

- Organistaion of the readout/electronics
- Determining the Bad Channels
- Determining the Pedestals
- Future plans

Organisation of the Readout Electronics



- One ECAL crate with 21 slots (0-20)
- Three of these slots (7, 15 & 19) contain Calice Readout Cards (CRCs).
- Each CRC contains 8 FE FPGAs. Not all appear to be connected to slabs.
- Each FE deals with 12 VFE chips (0-11).
- Each VFE chip deals with 18 channels (0-17).
- Therefore, each FE deals with 216 channels.

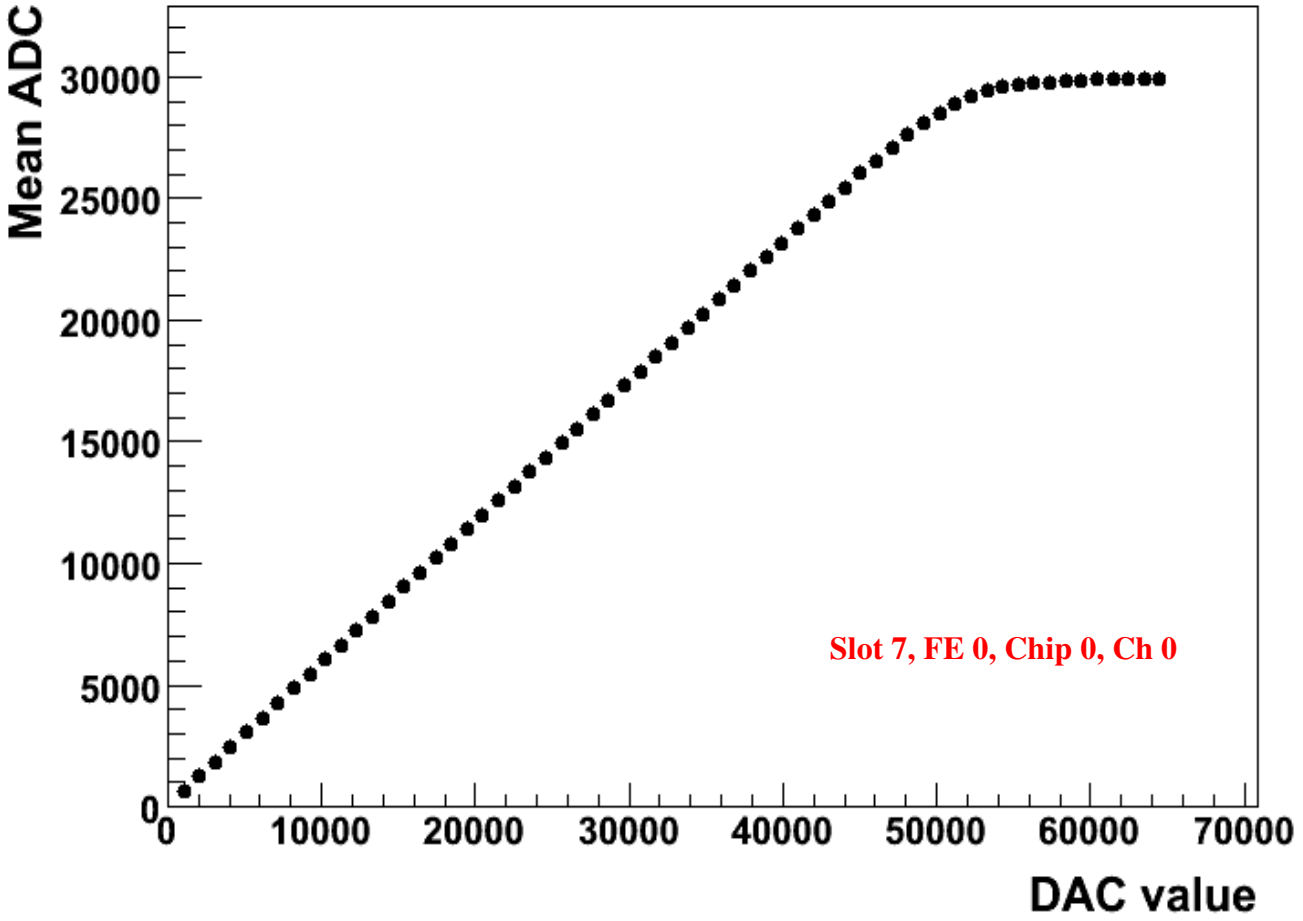
Determination of Bad Channels and Pedestals

- The goal here is to develop an (automated) calibration procedure.
- Shift crew could periodically run a special preconfigured *calibration run.* An automated analysis is then performed upon the collected calibration data to allow bad channels to be found and pedestals determined (amongst other things no doubt).
- Allows good calibration of the system and the information can be incorporated in to the simulation software (via Marlin Processor for example).
- Work is underway in developing such a calibration procedure.
- Paul recently took a calibration run at DESY.
- Run 200062.
- I (with Paul's valuable help!) am developing the analysis procedure.
- This talk will discuss what's been done so far.

Calibration Run 200062

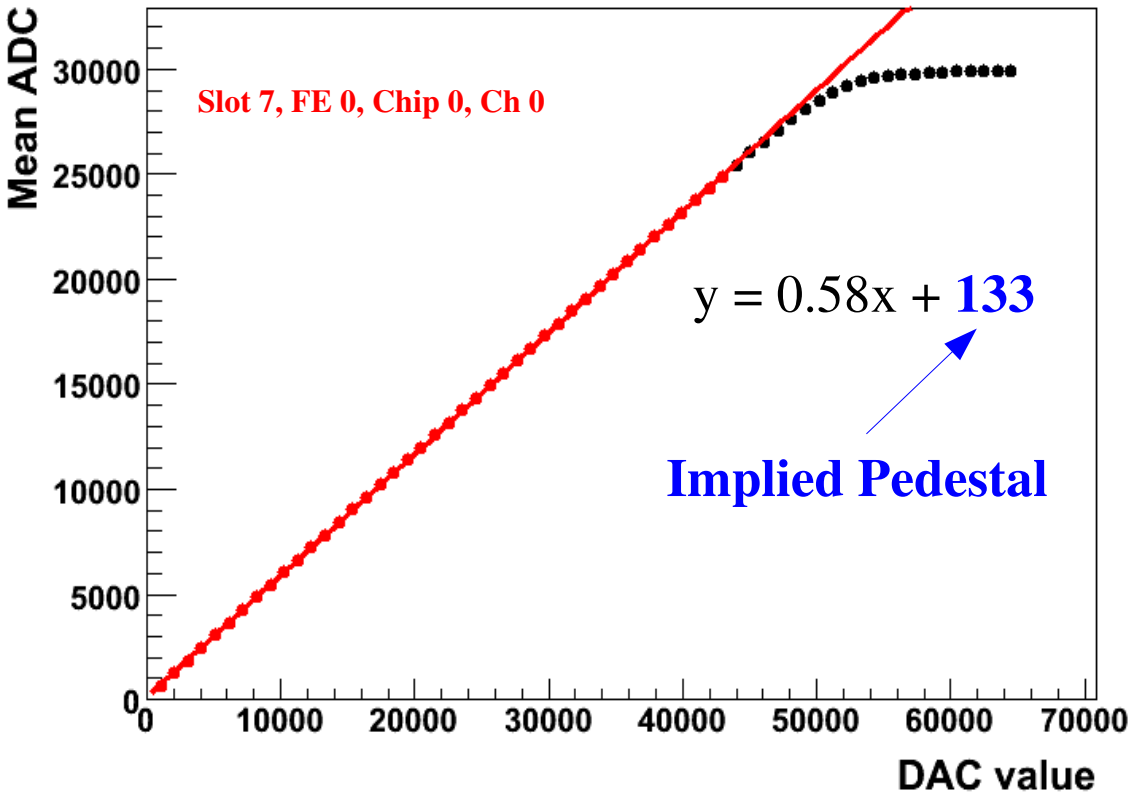
- Each VFE channel was pulsed with a calibration pulse (DAC) of varying magnitude.
- DAC size given by **i*1024** where **i=0,1,2, ... ,63**

Channel Diagnostics - Introduction



- A channel is diagnosed by plotting the mean ADC value for each DAC value.
- A healthy channel is characterised by a linear response of the Mean ADC with increasing DAC value.
- Saturation occurs at a DAC value of ~50000 corresponding to a mean ADC of ~30000.

Channel Diagnostics - Fitting

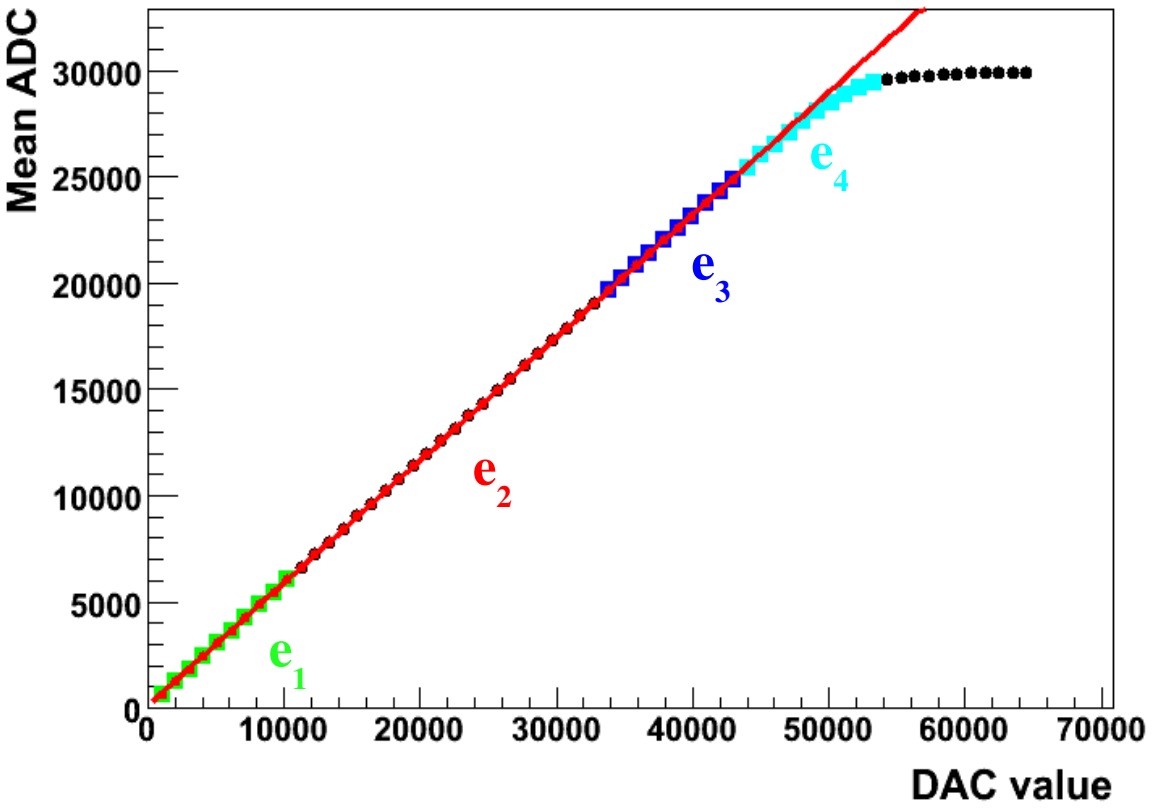


- Each channel is fitted with a first order polynomial.
- Linear regression formulae are used directly rather than fitting using ROOT.
- Much faster when the whole procedure has to be repeated 1000s of times.
- Only the first 42 points are fitted (red).

- To fit $f(a,b)=ax+b$ to straight line data use:

$$b=\frac{ss_{xy}}{s_{xx}} \qquad a=\bar{y}-b\,\bar{x} \qquad \text{where} \qquad ss_{xx}=\sum(x_i-\bar{x})^2 \qquad ss_{yy}=\sum(y_i-\bar{y})^2 \qquad ss_{xy}=\sum(x_i-\bar{x})(y_i-\bar{y})$$

Channel Diagnostics – Fit quality



- How rigorous is the fitting procedure. Need various tests. These tests not only test the quality of the fitting but also the quality of the channel itself.
- Calculate

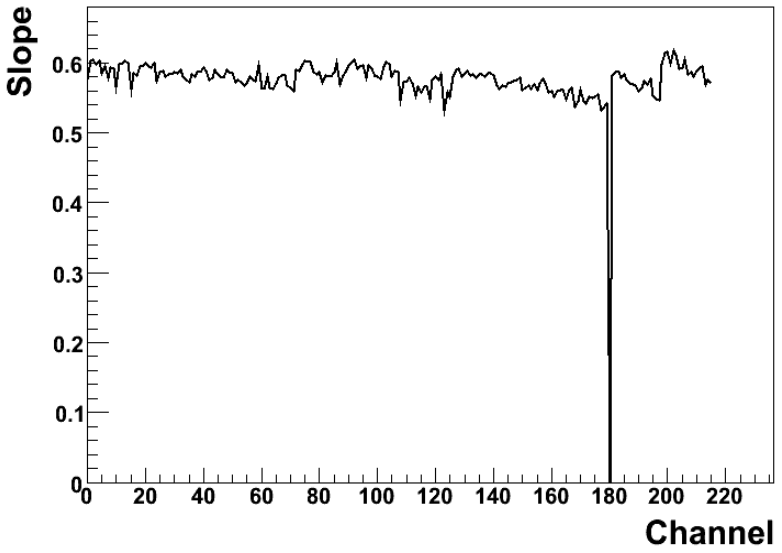
$$r^2 = \frac{ss_{xy}^2}{s_{xx}s_{yy}}$$

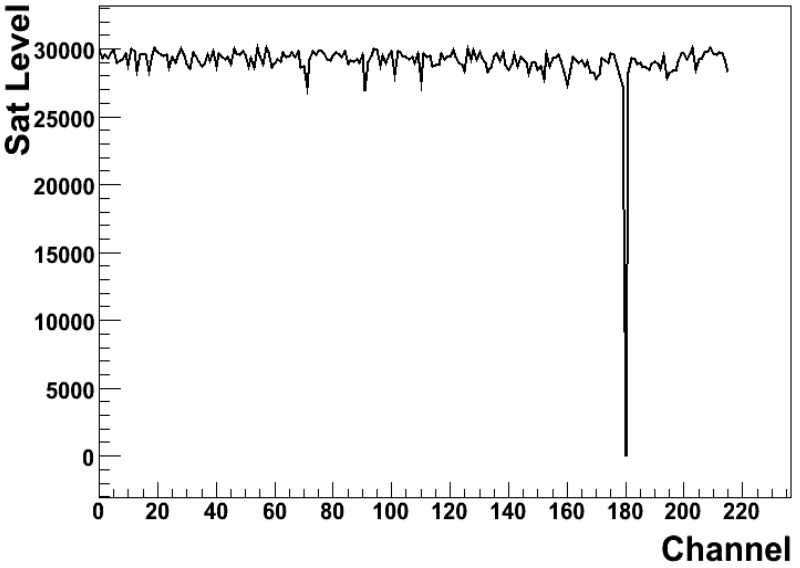
- Should be 1 if the fit is good.
- Next, consider the residuals in various regions.

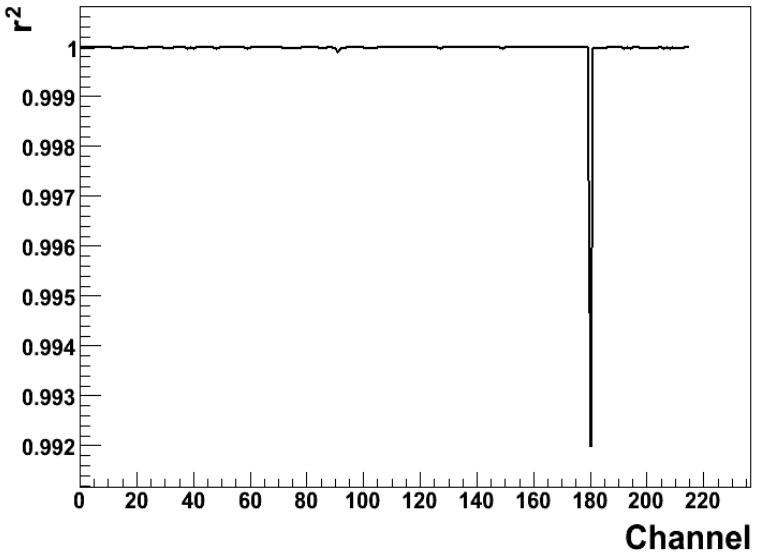
- e_1, residuals for the first 10 fitted points. Should be **~0** (test for linearity at low DAC values)
- e_2, residuals for the all fitted points. Should be **~0** (test for linearity across the entire fitted range)
- e_3, residuals for the last 10 fitted points. Should be **~0** (test for linearity at high DAC values)
- e_4, residuals for the next 10 points after the last fitted point. Should be **>0** (test for saturation in the expected region)

Channel Diagnostics – Study of Slot 7, FE 0

- Let's look at all channels in one FE. Say, Slot 7, FE0.

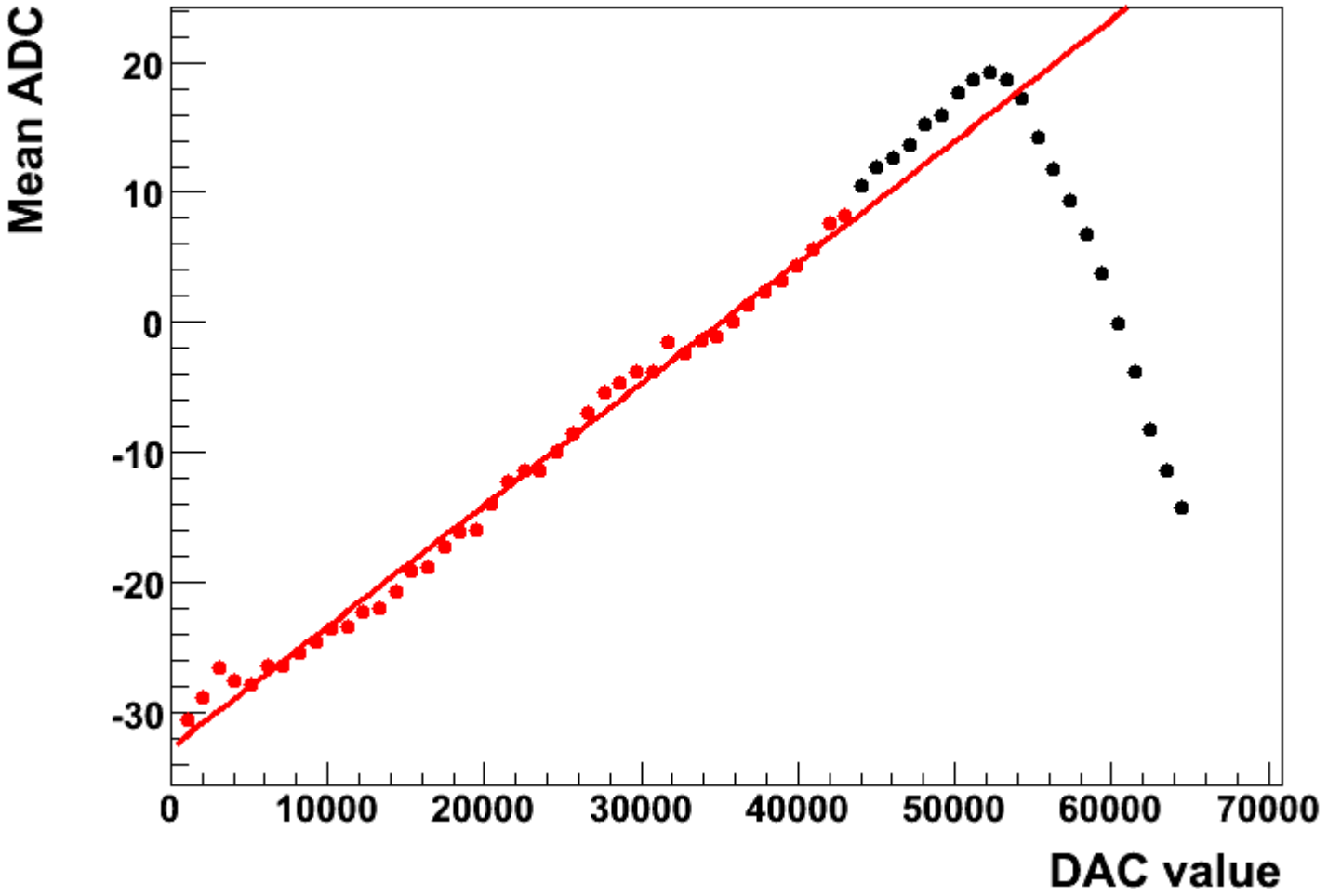






- 180 looks like a Bad Channel
- Let's take a closer look at 180 ....

Channel Diagnostics – Study of Slot 7, FE 0, Channel 180



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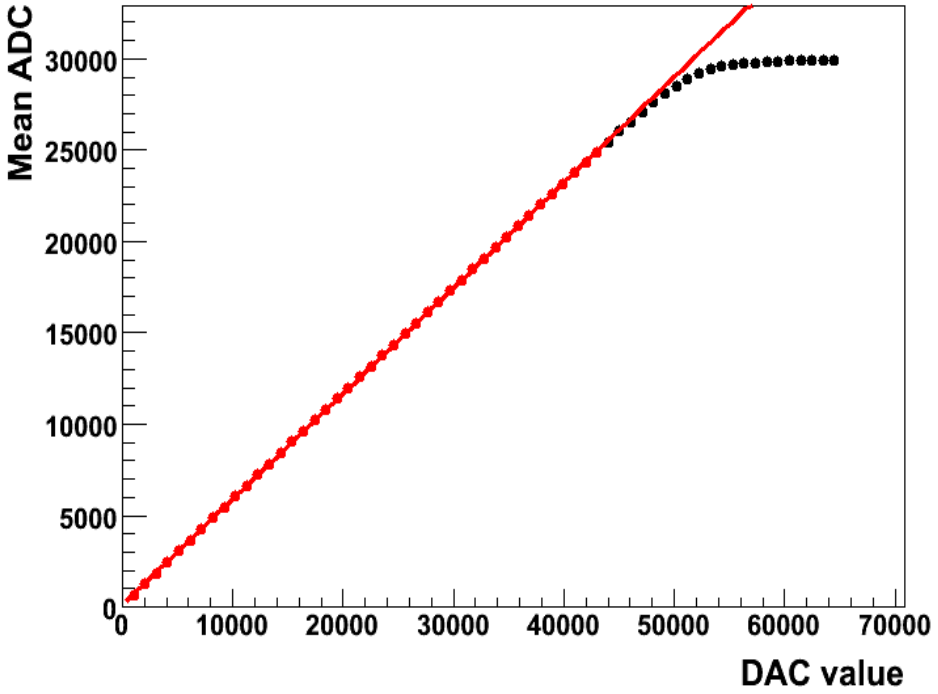
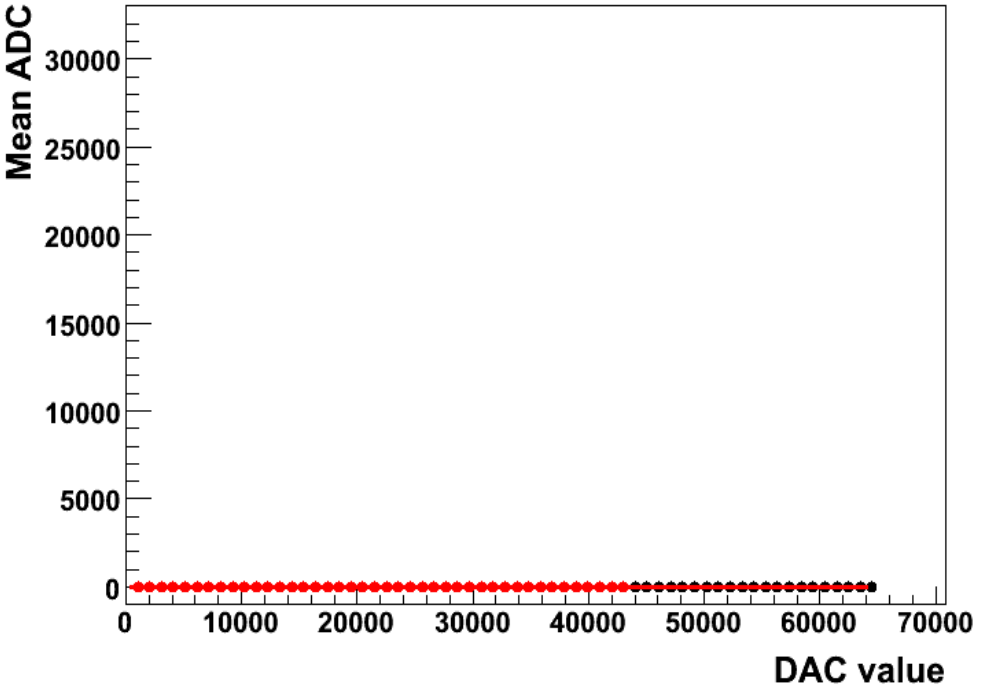
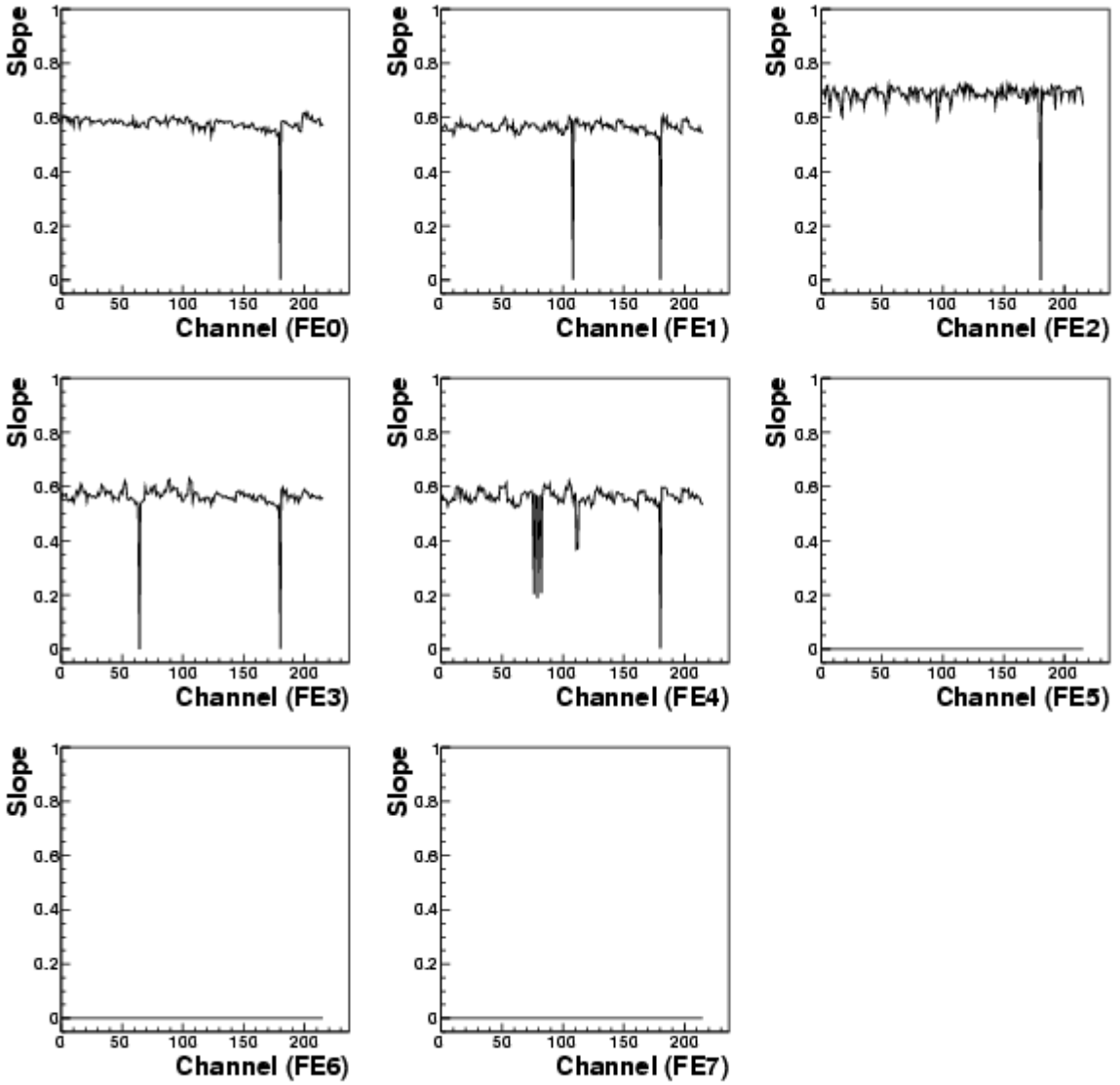
Channel Diagnostics – Study of Slot 7, FE 0, Channel 180





- Channel looks dead!
- Now let's look at the entire readout ....

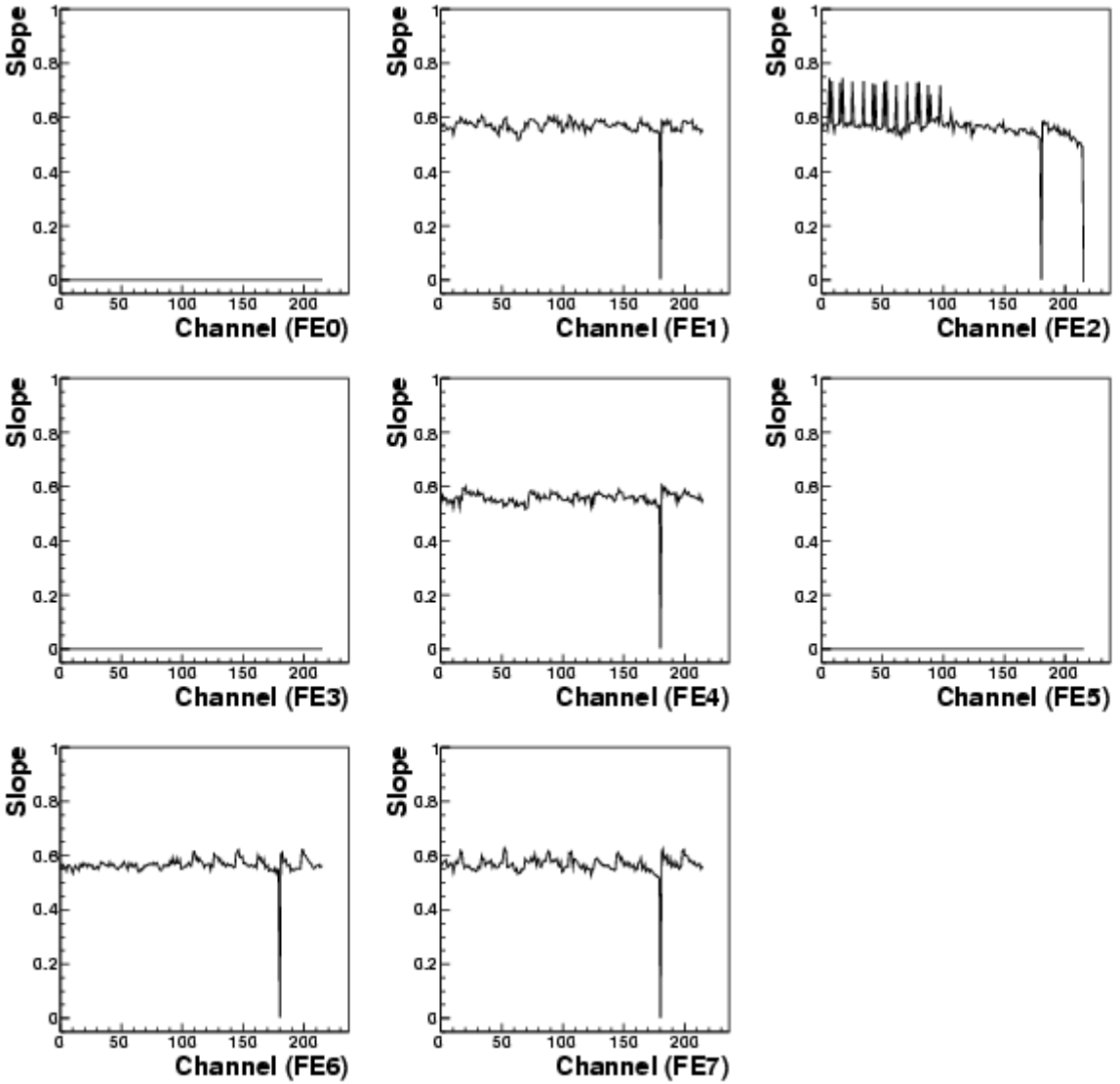
Channel Diagnostics – Study of Slot 7



Suspicious looking slope values. We'll come back to this.

- Not all FEs are active.
- Possible bad chip in FE4.

Channel Diagnostics – Study of Slot 15



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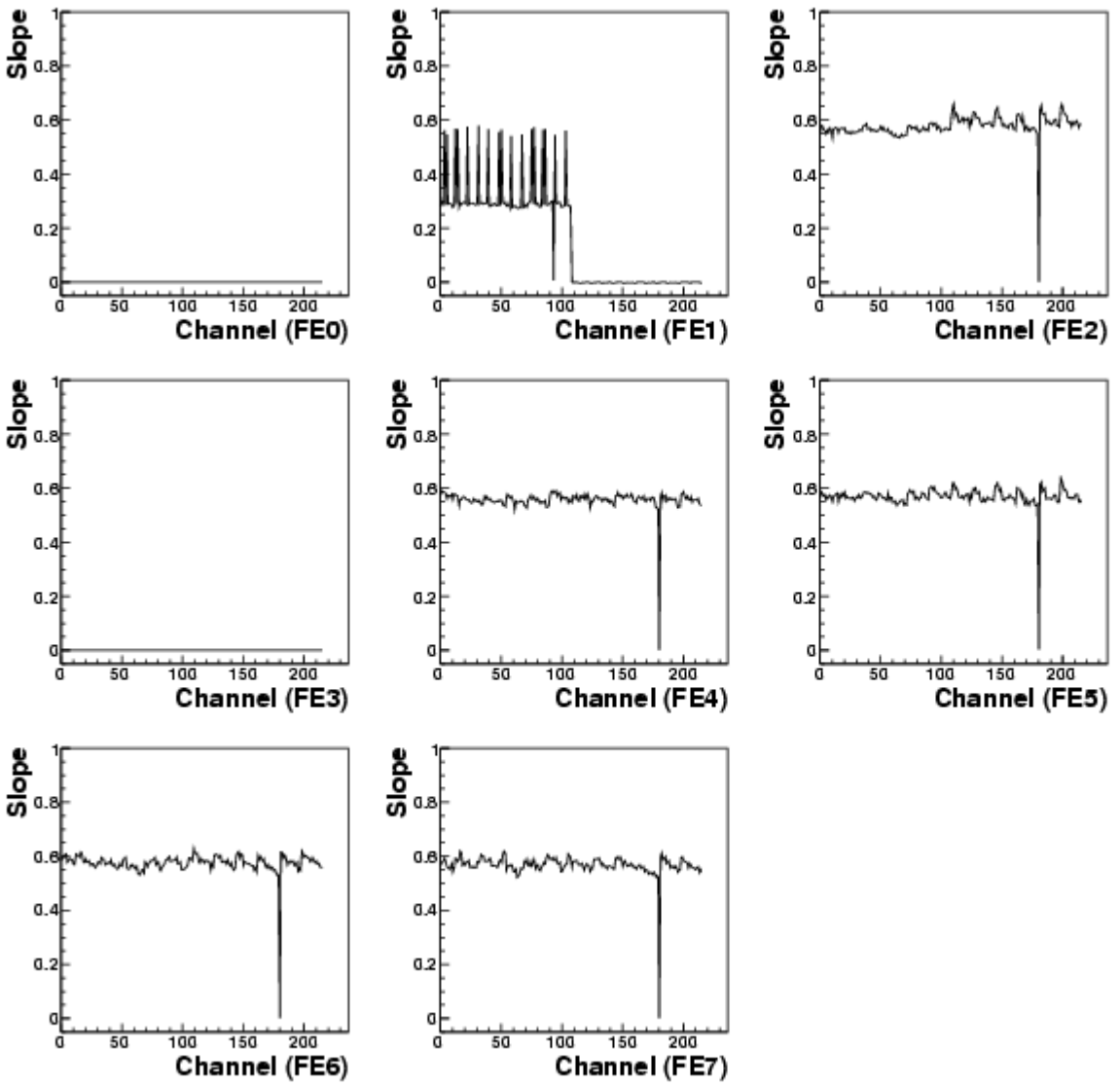
Channel Diagnostics – Study of Slot 19



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Channel Diagnostics – Summary

- Firstly, there is far too much information on this topic to show it all during this talk.
- Website has been set up at

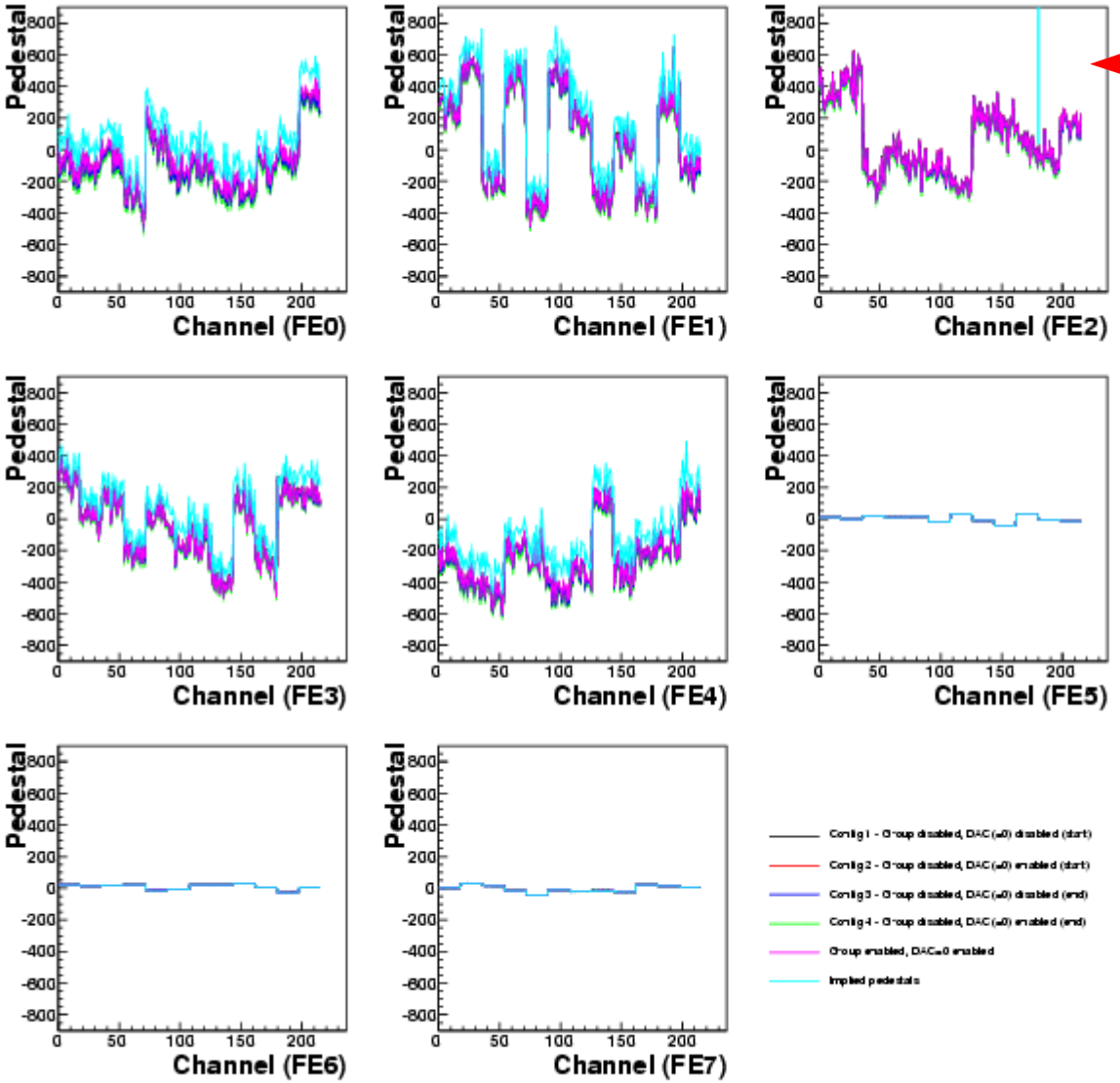
http://www.hep.ucl.ac.uk/~cta/calice/bad_channels/bad_channels.html

- This site shows all the plots that have been produced during the study presented in this talk (for all channels).
- Must decide on the criteria to be used to label a channel as bad.
- Then a list of bad channels can be added to the website. After each calibration run, the website can be automatically updated with a list of bad channels.

Pedestals

- Various methods of measuring the pedestal in each channel have been used
- The pedestals were measured:
  - At the beginning of the run
    - With the Group disabled and the DAC disabled.
    - With the Group disabled and the DAC enabled.
  - At the end of the run
    - With the Group disabled and the DAC disabled.
    - With the Group disabled and the DAC enabled.
- The pedestals were also measured with the Group enabled and the DAC enabled (and set to 0).
- In addition the implied pedestals were measured by taking the intercept of the straight line fits, discussed in the last section.
- These are all just slightly different ways of measuring the pedestal and they should give consistent results.

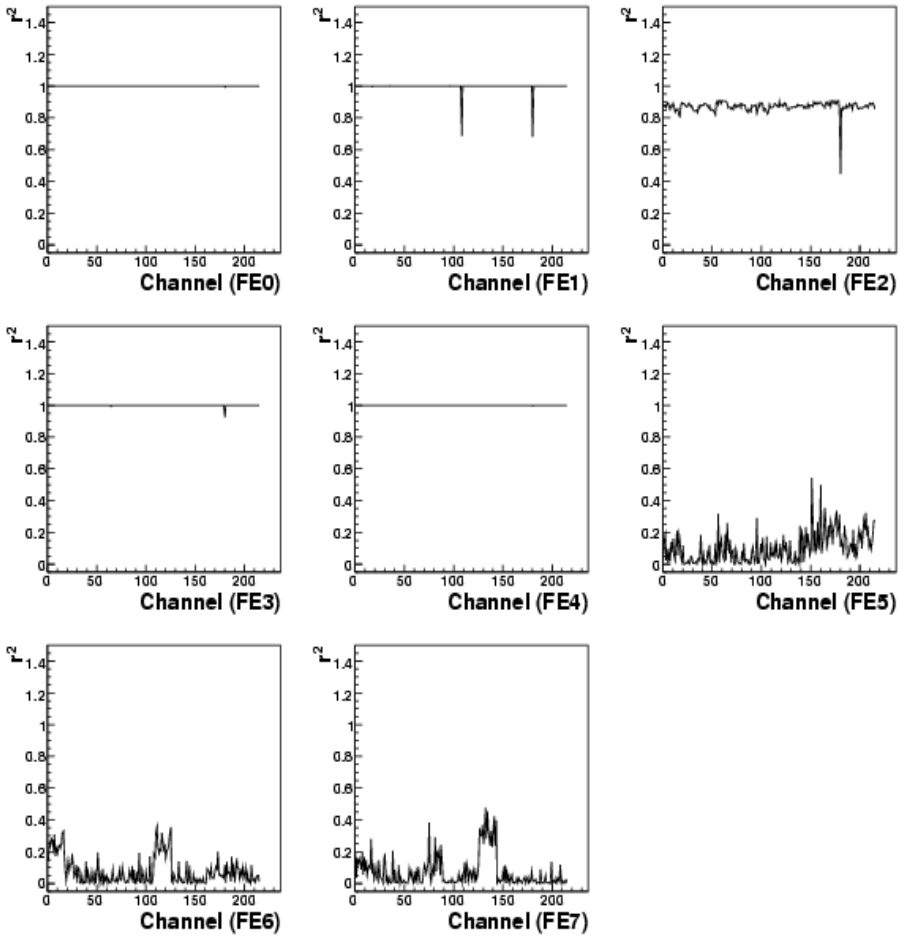
Pedestals – Slot 7



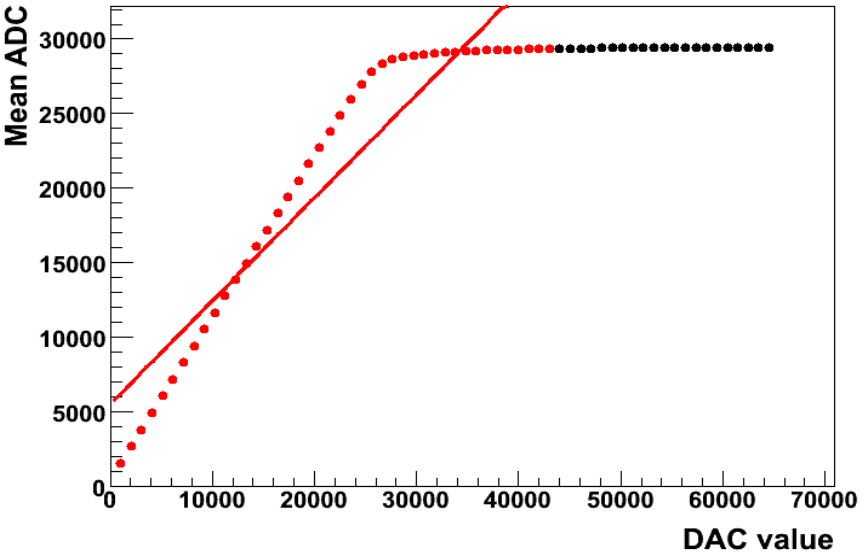
This was the FE with the suspicious looking slope values. The implied pedestals are huge.

- Noticeable chip-to-chip variation.
- Implied pedestals seem to be consistently higher than the other measures.

Fit qualities– Slot 7

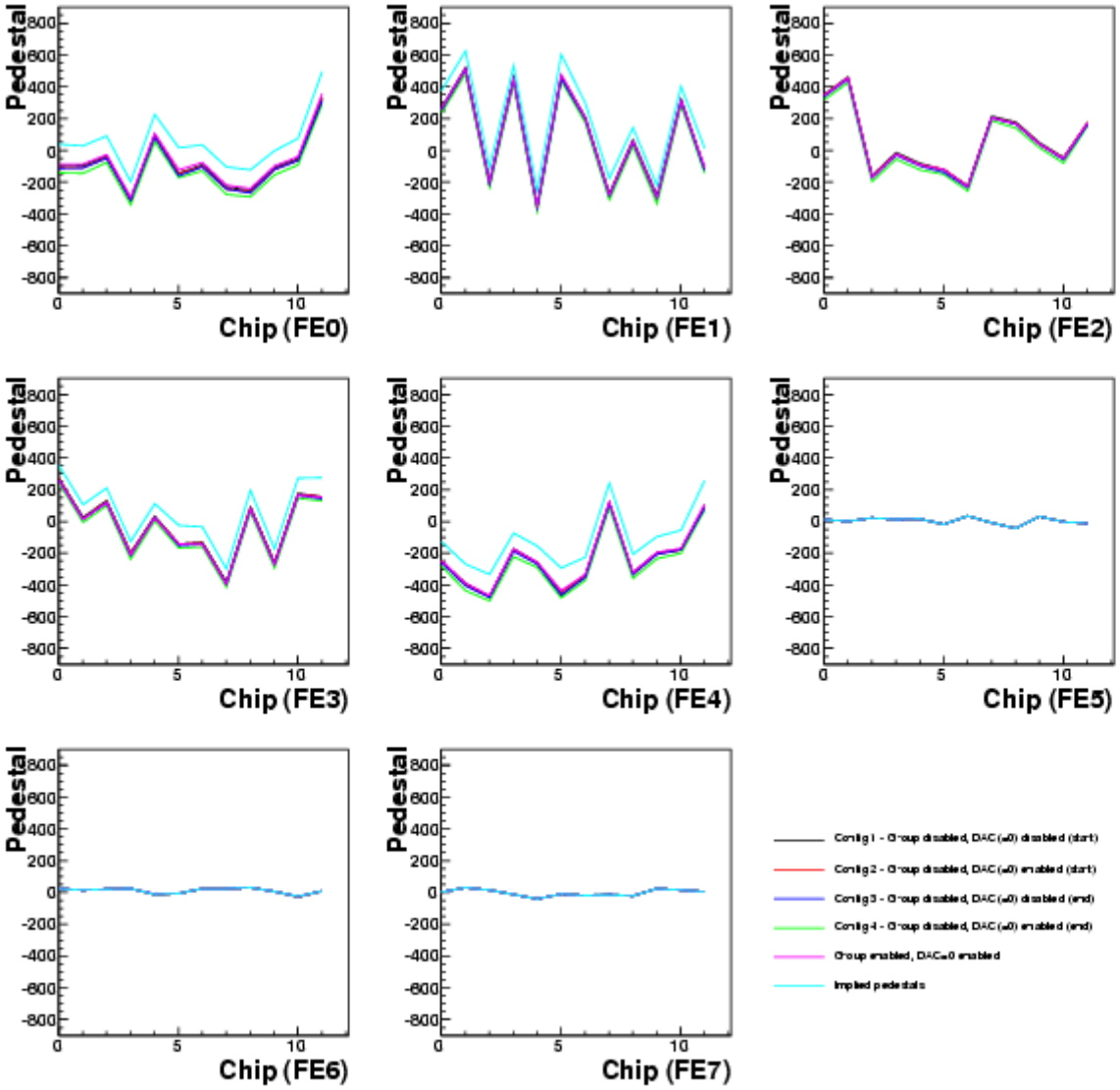


Let's look at channel 0 of FE2



- Looks like the channels are too sensitive in FE2.

Chip-by-Chip Pedestals – Slot 7



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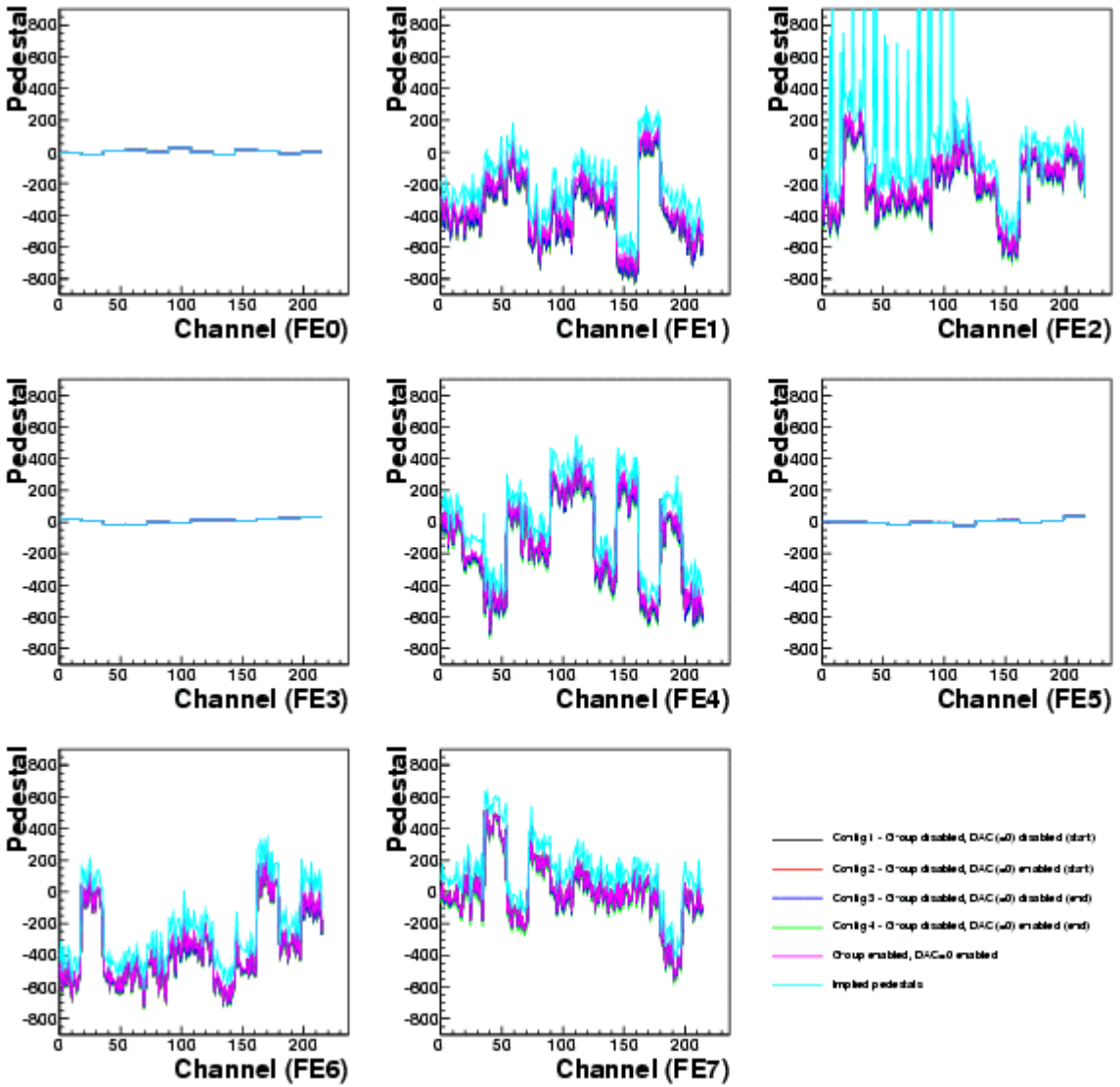
Pedestals – Slot 15



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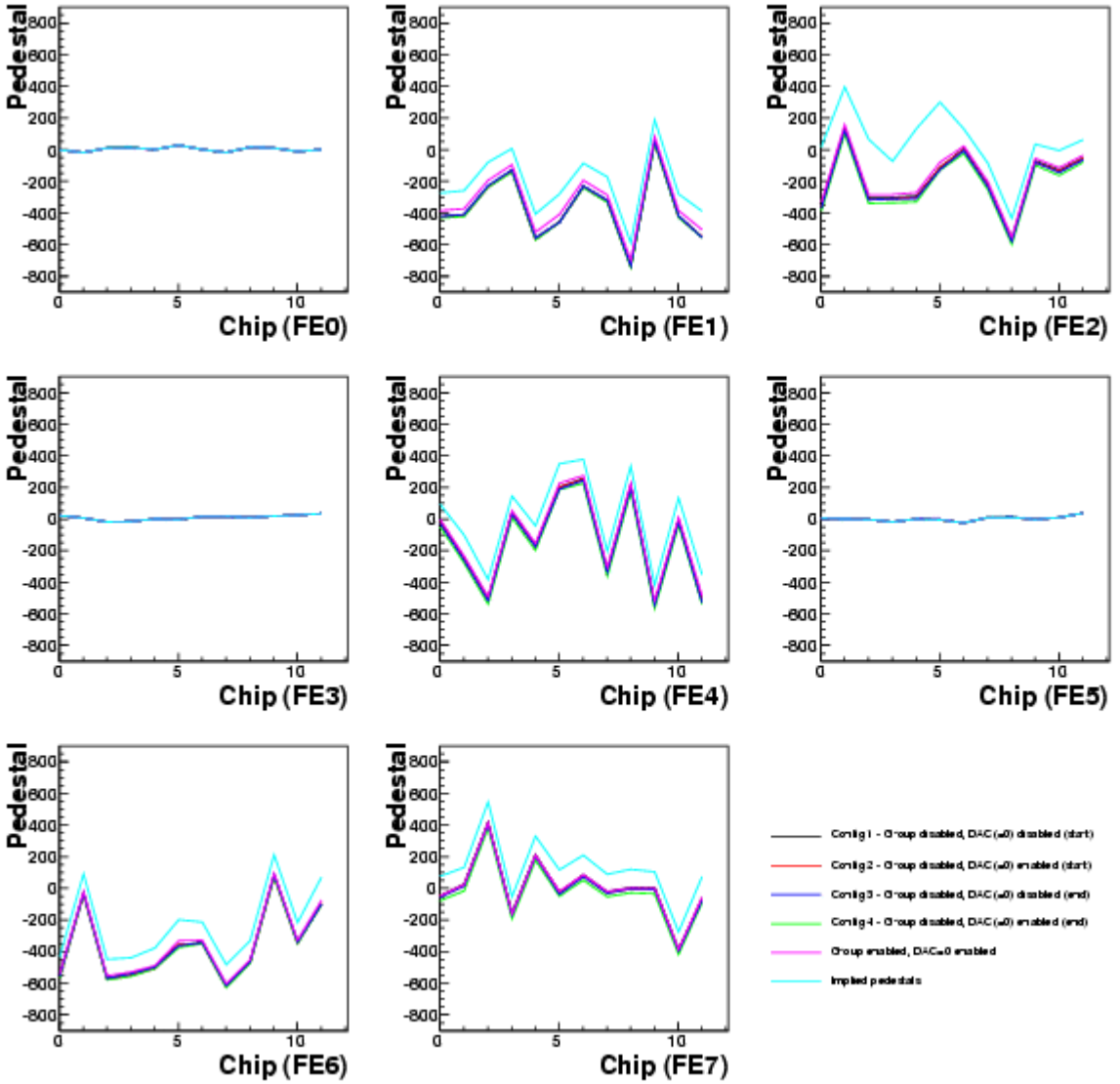
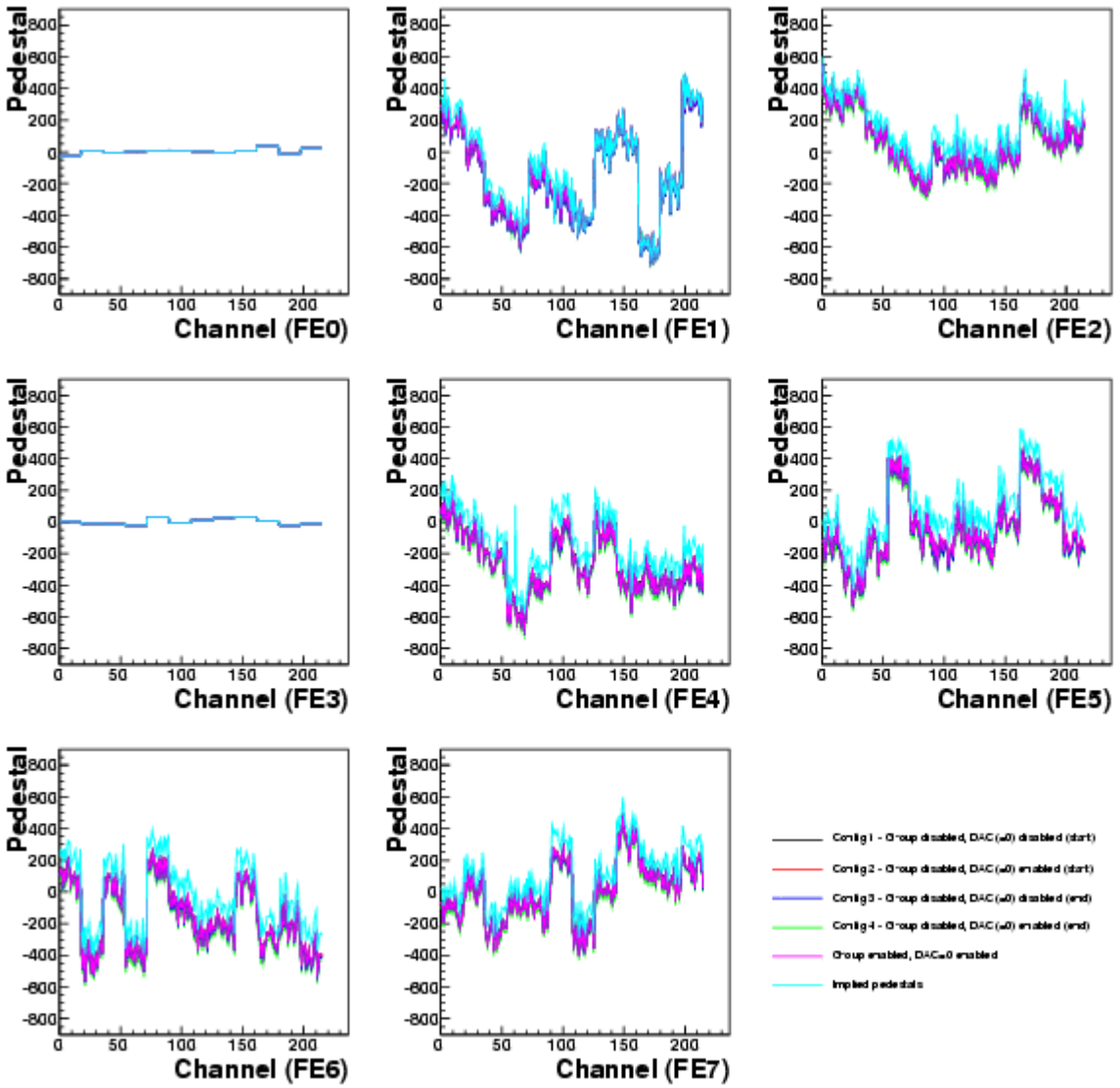
Chip-by-Chip Pedestals – Slot 15



Pedestals – Slot 19



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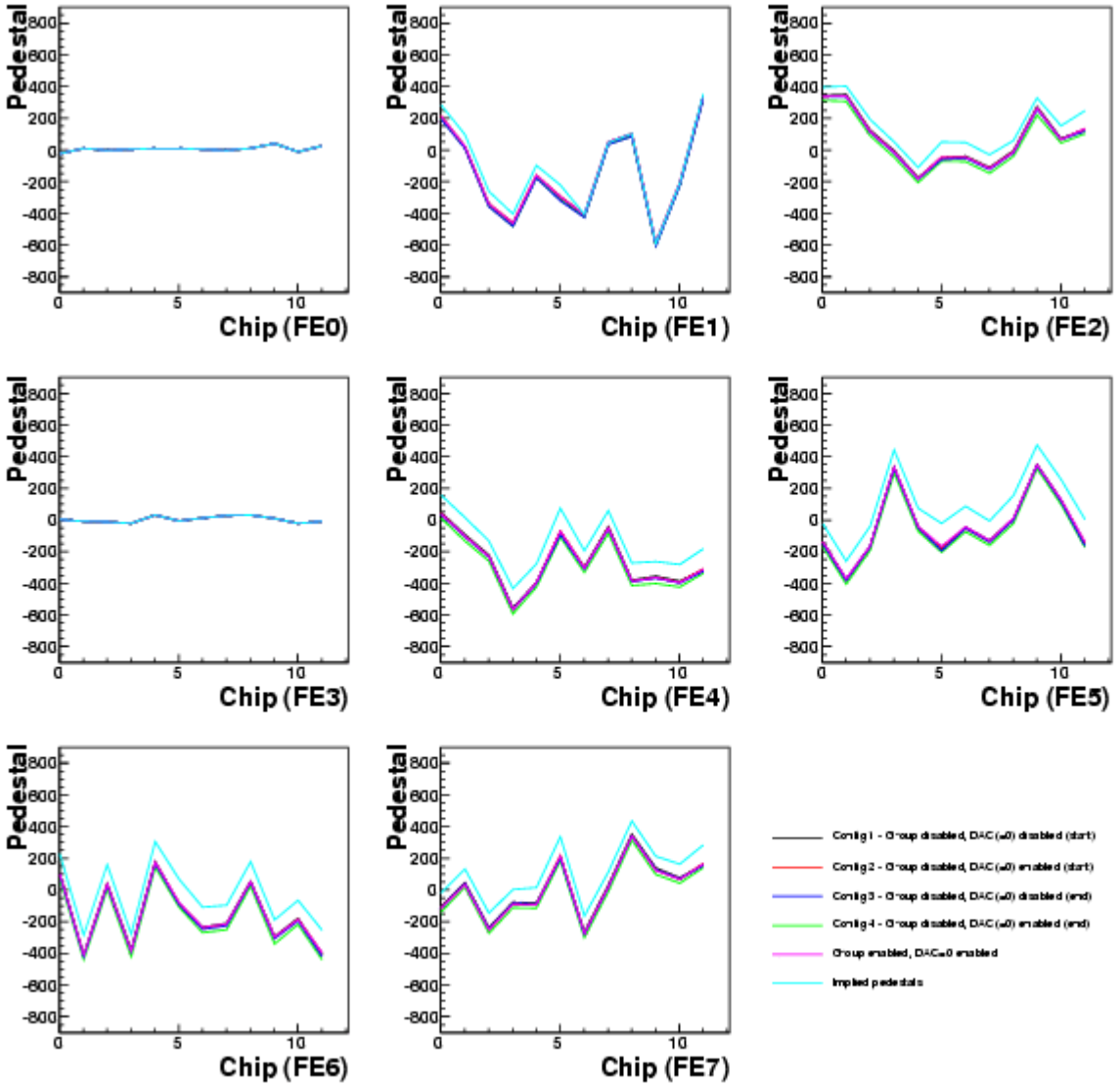
Chip-by-Chip Pedestals – Slot 19



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Summary

- Good progress made in the analysis of bad channels and pedestals.
- Need to specify the criteria which defines a channel as bad.
- Need to make the fitting more flexible so that it can deal with FEs such as FE2 of slot 7.
- Website has been set up to contain all of the bad channel and pedestal information.
- Why are the implied pedestals greater than the explicit pedestals?

Future work

- Address the issues above.
- Study the pulse shapes (HOLD).
- Study cross-talk in the system.
- Looking, ultimately, to establish a robust calibration procedure.
- ... and incorporate findings in the simulation of the test-beam data.